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(54) Circuit device for suppressing the dependence from temperature and production process variables of the transconductance of a differential transconductor stage.

(57) A circuit device for suppressing the dependence on temperature and production process variables of the transconductance of a differential transconductor stage incorporating a polarization circuit, comprises a negative feedback loop (1) being closed across an output (U) of the stage (2) and an input of the polarization circuit (3) and including a current generator (I2), capacitor (C), and at least a transistor (M).

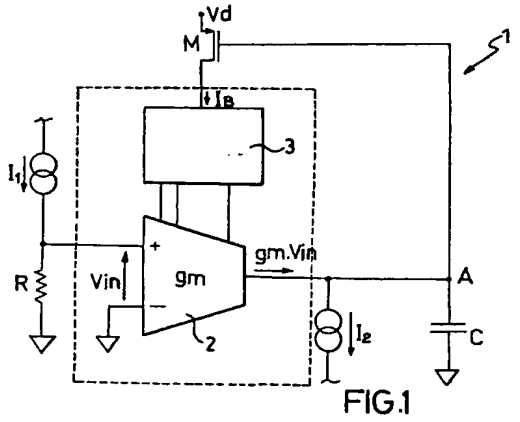

FIG.1

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This invention relates to a circuit device for suppressing the dependence from temperature and production process variables of the transconductance of a differential transconductor stage incorporating a polarization circuit.

The invention is particularly, but not exclusively, concerned with continuous-time monolithic filters, and the description that follows will make reference to this field of application for convenience of illustration.

As is known, of the many techniques which have been proposed heretofore for making continuous-time monolithic filters, a technique which uses a transconductor differential stage as the base block for the filter is gaining increasing acceptance. Associated with the stage is, of course, an appropriate polarization circuit.

Such a technique has proved specially effective in high-frequency applications. However, transconductor filters also have a drawback in that the transconductance value gm of the differential stage is tied to the operating temperature and the process of monolithic integration involved by the circuit fabrication.

In addition, the transconductance value is also dependent on a supply current Ib to the polarization circuit associated with the differential stage.

The variability of the transconductance gm with the above parameters adversely affects the width of the filter pass band, restricting its performance esepecially at high frequencies.

The underlying technical problem of this invention is to provide a circuit device which has such structural and operational features as to suppress the dependence on temperature, and on the integration process variables, of the transconductance of a transconductor stage, thereby overcoming the limitations with which prior devices have been beset.

Another object of the invention is to provide a circuit device which allows the user to control and set the value of said transconductance to suit the applicational requirements of the differential stage.

The solutive idea on which this invention stands is one of so adjusting the value of the supply current Ib to the polarization circuit associated with the differential stage as to accommodate any unbalance effects on the transconductance from temperature and process variables.

Starting from this solutive idea, the technical problem is solved by a circuit device as defined in the characterizing part of Claim 1.

The features and advantages of the device according to the invention will be apparent from the following detailed description of an embodiment thereof, given by way of example and not of limitation with reference to the accompanying drawings.

In the drawings:

Figure 1 is a diagram depicting the circuit device of this invention;

Figure 2 is a more detailed diagram of the device shown in Figure 1;

Figure 3 shows a modified embodiment of the device in Figure 1;

Figure 4 is a diagram illustrating an exemplary application of the inventive device; and

Figure 5 and 6 are respective diagrams showing details of the device in Figure 1.

With reference to the drawing figures, generally and schematically shown at 1 is a circuit device embodying this invention and effective to suppress the dependence on temperature and variables of the production process of the transconductance gm of a so-called transconductor stage 2. The device 1 is of the monolithic type.

Dependence on production process variables means here the effect on transconductance of the process steps whereby the transconductor circuit is made using conventional very large scale integration techniques.

The structure of stage 2 is known per se and from pertinent technical literature. This stage 3 is fabricated using a mixed technology, in that it includes both bipolar transistors and field-effect MOS transistors.

Associated with the stage 2 of figure 1 is a polarization circuit 3 connecting said stage to a positive voltage supply pole Vd. In addition, the inverting (-) input of stage 2 is connected directly to a reference potential, while the other, non-inverting (+) input is connected both to the pole Vd, via a current source I1, and to a reference potential via a resistor R.

Across said inputs, a voltage signal Vin is applied to produce, on an output U of stage 2, a current signal resulting from the product gm*Vin, where gm is the transconductance value of stage 2.

Advantageously, the device 1 of this invention comprises a negative feedback loop having a uniquely simple structure. This loop is closed across the output U of stage 2 and an input of the polarization circuit 3. Incorporated to the feedback loop are: a current generator I2, a capacitor C, and a transistor M of the MOS type.

Making reference to figure 1, it may be noted that the output U of the stage 2 is connected to the reference potential through the parallel connection between the generator I2 and the capacitor C. The connection point is indicated as node A and is connected also to the gate electrode G of the transistor M.

This transistor M is of the p-channel type, and has its source electrode S connected to the voltage pole Vd and its drain electrode D connected to the input end of the polarization circuit 4 to supply said circuit with a current Ib.

As previously mentioned, the transconductance gm is also dependent on the value of the supply current Ib to circuit 3. Assuming this dependence to be of a proportional nature, it is found that: gm = Kv*Ib

where Kv is a proportionality constant >0.

With the additional assumption that:

I1 = Vb/R and I2 = Vb/Re

where Vb is a voltage derived from the supply voltage, e.g. Vb = Vd/2, and Re is an external resistance to the integrated circuit whose value is accurately predetermined, the following relation can be obtained:

(1) Vin = R*I1 = Vb

Illustrated in Figure 6 is an embodiment of the generator I1, incorporating an operational amplifier 5 which has a non-inverting (+) input supplied with the voltage Vb and the output connected to the gate electrode G5 of an n-channel MOS transistor M5. The inverting (-) input of amplifier 5 is instead connected to the source S5 of transistor M5, which is also connected to a reference potential through the resistor R.

Current I1 flows through transistor M5 from the drain D5 to the source S5.

The feedback loop of device 1 acts on the voltage appearing at node A to equalize the current output from stage 2 to current generator I2, and hence, such that:

(2) gm*Vin = I2

but when the value of Vin from the previous relation (1) is substituted in this relation, then it is found that:

(3) gm*Vb = I2 = Vb/Re

whence gm = 1/Re

Consequently, the feedback loop brings the circuit node A to such a voltage level as to bias to the active zone the transistor M, which will supply the current Ib directly into the polarization circuit 3 of stage 2. The latter is biased to the linear operation zone by effecting a linear voltage-to-current conversion and achieving a transconductance value gm = 1/Re.

The external resistance Re has a value which is defined by the user and is only required to be a temperature-wise stable kind because it is on it that the transconductance value gm obtained through the inventive device is dependent.

Shown in Figure 5 is an embodiment of the generator I2 which includes an operational amplifier 7 having its non-inverting (+) input supplied with a Vb voltage value and its output connected to the gate G7 of a MOS transistor M7. The source electrode S7 of this transistor is connected to the inverting (-) input of amplifier 7, and to a pin 8 of the integrated circuit incorporating the device of this invention.

Connected across said pin 8 and the reference potential is the external resistance Re.

In the embodiment described with reference to Figure 1, the dynamic resistance across the node A and the reference potential is theoretically an infinite value. However, to ensure stability of feedback loop, the provision of capacitor C is required to introduce in the frequency response a dominant pole useful to make sufficiently low the unitary gain frequency of the feedback loop, if compared to those of the other secondary poles in the feedback loop.

The capacitance of capacitor C is preferably lower than 30 pF, that is, enough to allow integration thereof.

In a preferred embodiment shown in Figure 3, the current source or generator I2 is associated with a DAC (Digital to Analog Converter) converter 10 having a plurality n of digital selection inputs a0, a1,...,an. Each of these inputs represents one bit of an n-bit digital word selected by the user, which word allows the value of a multiplier parameter α to be defined which turns the current generator I2 into a variable current generator having a value of α*I2.

The value of α is proportional to the input values in accordance with the following expression:

$$\alpha \cong a_0*2^0 + a_1*2^1 + \ldots + a_n*2^n$$

Revising relations (1) and (2) in the light of the variable current generator α*I2, it is found that:

(4) gm*Vin = gm*Vb = α*I2 = α*Vb/Re

whence:

(5) gm = α/Re

The transconductance value gm, which is made independent of temperature and process variables by means of the circuit loop according to the invention, can be controlled and set by the user defining the parameter α.

The device of this invention has proved effective even where plural transconductor stages were to be operated.

Figure 4 shows an embodiment of a circuit structure wherein plural stages 4, each having a transconductance value which is nominally the

same as that of stage 2, are arranged in parallel and supplied through the same polarization circuit 3.

Here again, the feedback loop 1 associated with stage 2 and circuit 3 can accommodate the effects on transconductance of all stages 2 and 4, as due on temperature and process variables.

For completeness of discussion, a detailed example of the best mode currently contemplated of implementing the inventive device shown in Figure 2 will be given herein below.

The transconductor stage 2 is a differential type comprising an input portion formed of a pair of n-channel MOS transistors M1, M2 which have their source terminals in common and define a circuit node H. Connected between said node and a reference potential is a current source A1.

The gate terminal G1 of the first-named transistor, M1, constitutes a non-inverting (+) input for the differential stage. The gate G2 of the second-named transistor, M2, constitutes the inverting (-) input, and the voltage Vin is applied across said inputs.

To avoid distortion phenomena in the output current, the input voltage Vin is applied within the transconductor linear field through a resistive divider connected across said inputs of stage 2 and composed of a pair of resistors having a value of R/2.

To the junction point of the resistors, a so-called common mode voltage Vcm is applied, with the current sources I1 connecting, on the one side, the non-inverting (+) input to the supply pole Vd, and on the other side, the inverting (-) input to a reference potential.

In this way, the input voltage Vin is made to coincide with the previously discussed value Vb, but disposed in an exactly differential manner relatively to the common mode voltage Vcm.

Stage 2 also includes an output portion comprising a pair of npn bipolar transistors Q1 and Q2 which have their bases connected to each other. These transistors are connected in the stage 2 in a cascode configuration, and the collector C2 of one Q2 of them constitutes the output terminal for the differential stage 2.

A third transistor, Q3, of the bipolar type has its base B3 connected to the bases B1, B2, and its emitter connected to the node H via a resistor R1.

A current mirror circuit 6 is adapted to supply to the output A the current value gm*Vin produced by the MOS transistors M1 and M2.

The gate G of the transistor M is connected to collector C2, which is also connected to the reference potential by the parallel of the variable generator α*I2 and capacitor C. The sourse S of the same transistor M is connected to the Vd pole.

Finally, the polarization circuit 3 comprises a group of three bipolar transistors Q4, Q5, Q6 having respective bases in common. The two first-named transistors Q4, Q5 in this group have emitters taken to a reference potential, each through a resistor R1, and the third-named transistor Q6 has its emitter connected to the drain of a MOS transistor M4 which has its source grounded and gate connected to a costant voltage generator V4.

A further MOS transistor M3 has its gate and source respectively connected to the collector and the base of the first-named bipolar transistor Q4. The gate G3 of this MOS transistor M3 is connected, moreover, to the drain D of transistor M and constitutes an input for the polarization circuit 3.

Claims

1. A circuit device for suppressing the dependence on temperature and production process variables of the transconductance of a differential transconductor stage incorporating a polarization circuit, characterized in that it comprises a negative feedback loop (1) closed across an output (U) of the stage (2) and an input of the polarization circuit (3), and including a current generator (I2), capacitor (C), and at least a transistor (M).

2. A device according to Claim 1, characterized in that said output (U) is connected to a reference potential through the parallel of said current generator (I2) and said capacitor (C), and to a gate electrode (G) of said transistor (M).

3. A device according to Claim 1, characterized in that said transistor (M) is a field effect transistor and is connected in the feedback loop (1) with respective drain (D) and source (S) electrodes arranged to interconnect the polarization circuit (3) and a supply voltage (Vd) pole.

4. A device according to Claim 3, characterized in that said transistor (M) is a p-channel type with a source electrode (S) connected to said voltage pole (Vd) and a drain electrode (D) connected to the polarization circuit (3).

5. A device according to Claim 1, characterized in that said current generator (I2) has a varying value.

6. A device according to Claim 1, characterized in that said current generator (I2) is connected to a digital-to-analog converter (10) having n digital selection inputs (a0,...,an) wherethrough

the user is enabled to define a multiplier parameter α whose value modulates that of the current generator (I2).

7. A device according to Claim 1, characterized in that said current generator (I2) includes an operational amplifier (7) having a non-inverting (+) input supplied with a predetermined voltage value (Vb) and an output connected to the gate (G7) of a MOS transistor (M7), with said transistor (M7) having a source (S7) connected to the inverting (-) input of the amplifier (7).

8. A device according to Claim 7, characterized in that said source (S7) is connected to a reference potential through a resistance (Re) having a stable value with temperature.

9. A circuit device for suppressing the dependence on temperature and production process variables of the transconductance of a plurality of differential transconductor stages (4) being supplied in parallel from a polarization circuit, characterized in that it comprises a negative feedback loop (1) closed across an output (U) of one (2) of said stages and an input of the polarization circuit (3) and including a current generator (I2), capacitor (C), and at least a transistor (M).

10. A device according to Claim 9, characterized in that said output (U) is connected to a reference potential through a parallel of said current generator (I2) and said capacitor (C), and to the gate electrode (G) of said transistor (M).

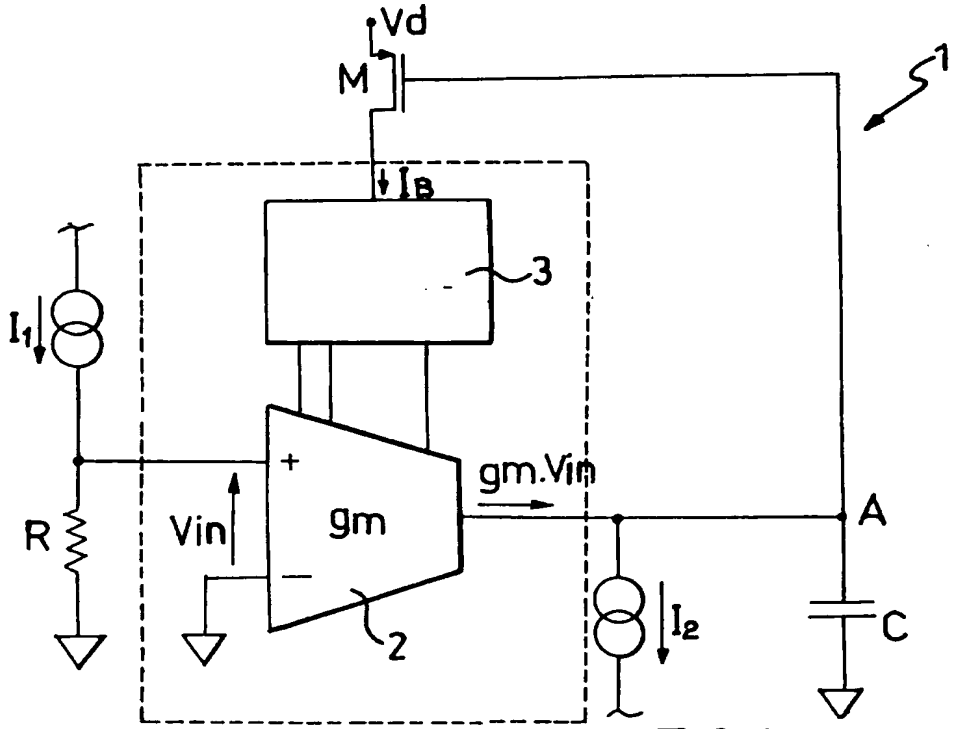


FIG.1

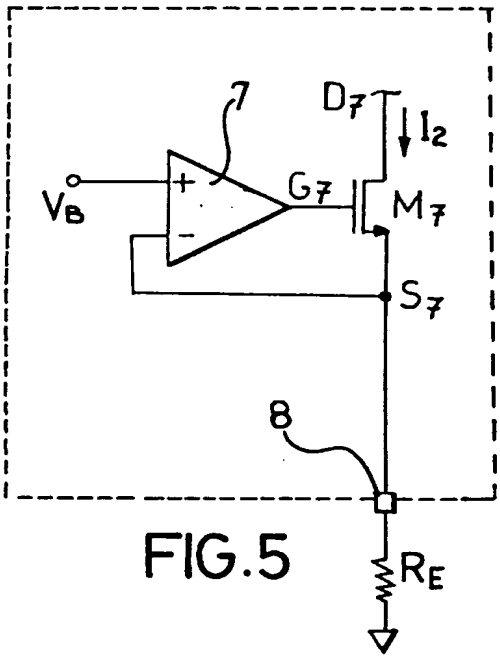


FIG.5

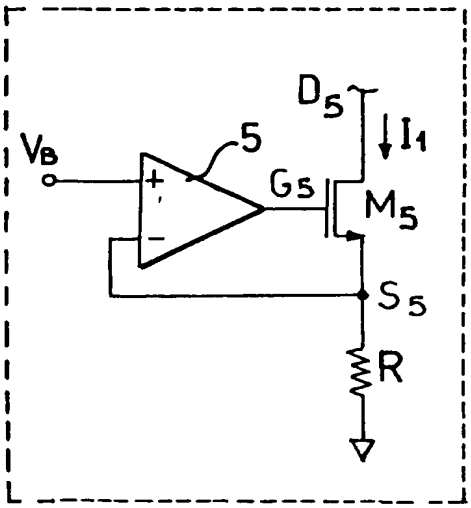
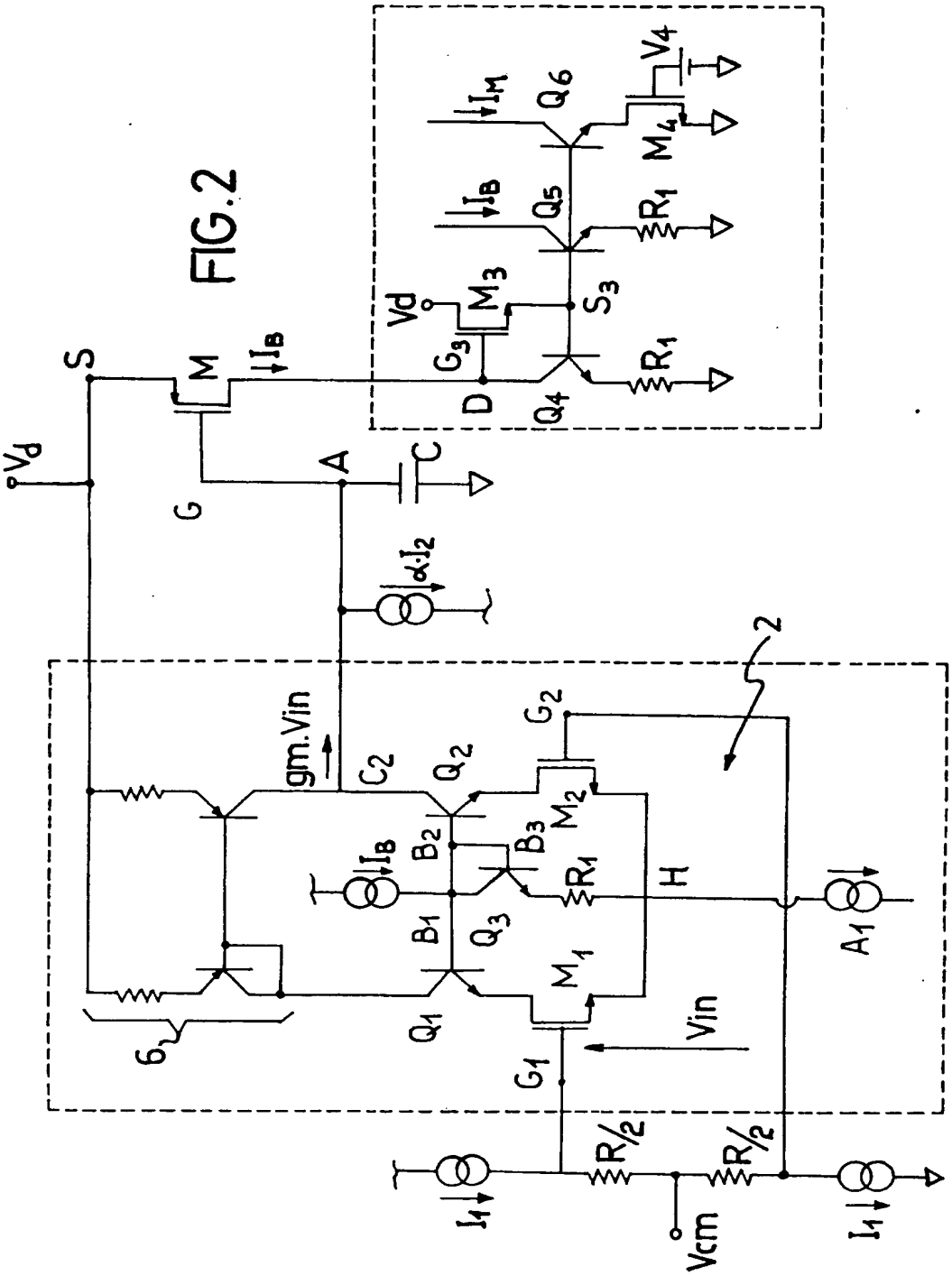


FIG.6

FIG.2


S
M
I_B
Vd
G
A
C
$\alpha \cdot I_2$
gm.Vin
C_2
Q_2
G_2
M_2
B_2
B_3
I_B
R_1
H
A_1
B_1
Q_3
M_1
Q_1
Vin
G_1
6
2
I_1
R/2
R/2
Vcm
I_1
I_M
Q_6
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Q_5
R_1
Vd
M_3
S_3
G_3
D
Q_4
R_1

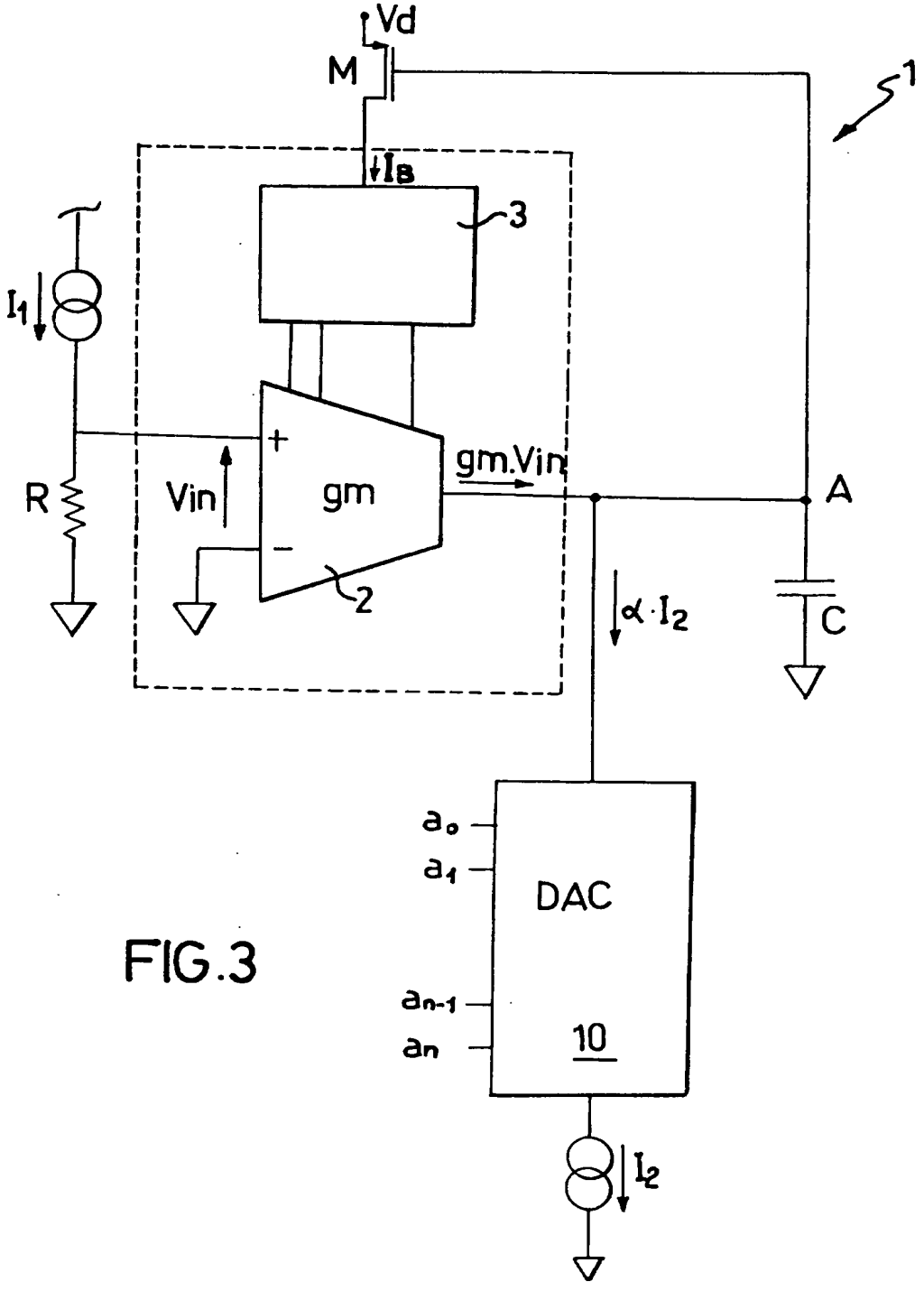
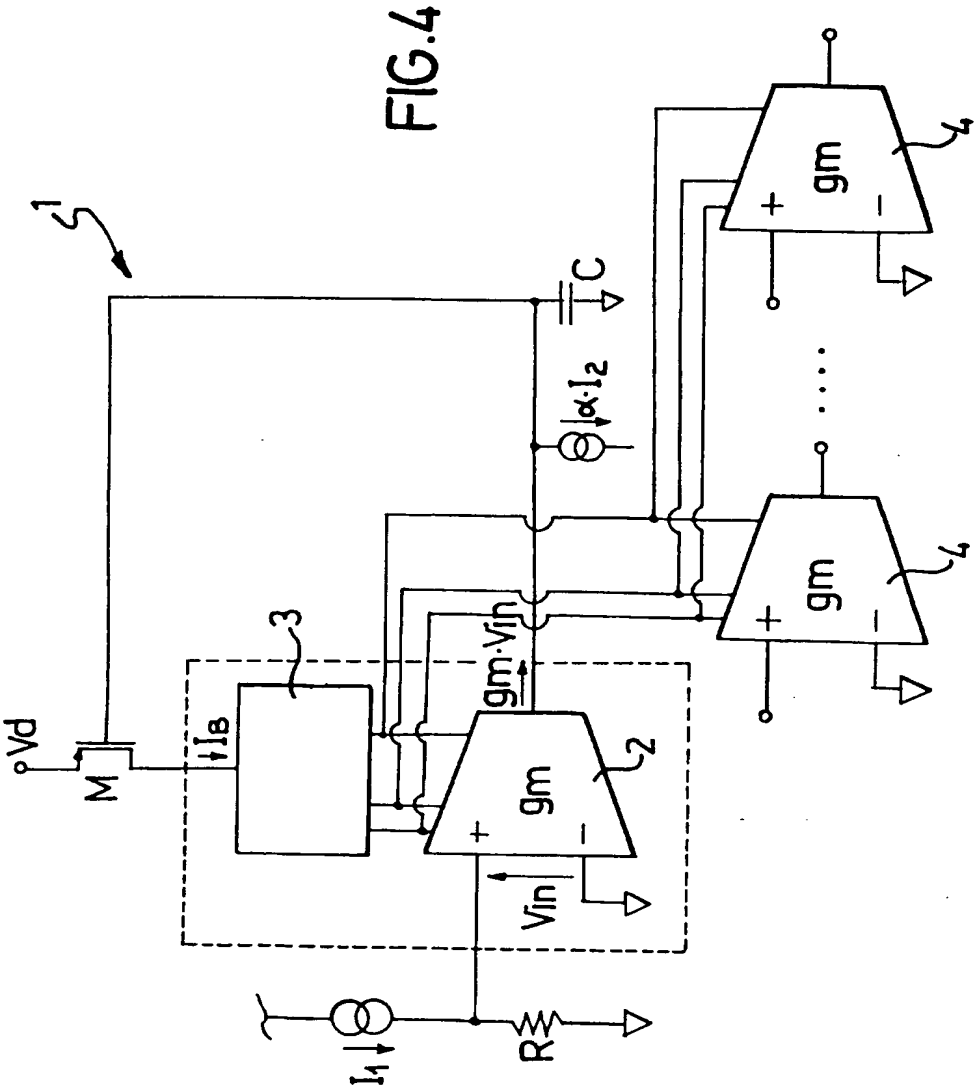

Vd
M
1
I_B
3
I_1
+
gm.Vin
R
Vin
gm
A
−
2
$\alpha \cdot I_2$
C
a_o
a_1
DAC
a_{n-1}
a_n
10
I_2

FIG.3

FIG.4



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EUROPEAN SEARCH REPORT

Application Number

EP 92 83 0140

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 723 108 (C.N.MURPHY ET AL) 2 February 1988 * column 1, line 1 - column 5, line 45; figures 1,2 *	1	H03H11/04
A		3-5	
A	IEEE 1983 INTERN. SYMP. ON CIRCUITS AND SYSTEMS; 2-4 MAY 1983; G.M.GLASFORD." CURRENT DEVELOPMENTS IN CMOS ..." P 1282-1285 * page 1283, column 2, line 16 - page 1284, column 2, line 38; figures 5,6 *	7,8	
A	1990 IEEE INT. SYMP. ON CIRCUITS AND SYSTEMS;1-3 MAY 1990;G.A.DE VEIRMAN et al FULLY INTEGRATED 5 TO 15 MHZ PROGRAMMABLE BIPOLAR BESSEL LOWPASS FILTER" P1155-1158 * page 1158, column 2, line 3 - page 1157, column 2, line 6; figures 1,5 *	9	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H03H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 NOVEMBER 1992	COPPIETERS C.

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